A Fast Settling, Low Phase Noise, Digitally Controlled 2.4GHz CMOS 12-bit ΣΔ Fractional-N Synthesizer with Programmable Step Sizes

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Abstract – **Frequency synthesizer has been a key element in various communication systems covering a wide range of applications. The requirements on step sizes, channel selection, offset in output frequency and frequency resolution vary with application, data transmission speed and data modulation scheme etc. The recent evolutions have encouraged development of integrated fractional-N synthesizer that features application versatility. A 2.4GHz CMOS 12-bit ΣΔ fractional-N synthesizer using 0.35μm CSM process is designed. Unlike to the conventional architectures, it is based on two input data words and features programmable step sizes (18.4kHz to 0.5MHz), programmable channels (64), programmable output frequency offsets (0 to 37MHz), 19mA current consumption @ 3V Supply, phase noise of -110 dBc/Hz @1MHz, settling time < 37μS, %32/33 DMP and 4.2mm² die area.**

I. INTRODUCTION

Evolutions in modern communication systems demand design solutions such as flexible Low Noise Amplifier for multi-bands receivers/Software Defined Radios, programmable VCO (Voltage Controlled Oscillator) for wide range of Local Oscillators and application versatile synthesizers particularly for multi-bands systems. The requirements of synthesizers on step size, resolution, channel selection and offset in output frequency vary with application. The conventional architectures for fractional–N synthesizers use one input data word providing hardware-fixed step size and do not meet such requirements [1-4]. Keeping in view the advantages of fractional-N synthesizers over integer-N synthesizers, above requirements and limitations of conventional architectures, programmable fractional-N synthesizers using digitally controlled data inputs seem possible solutions. This paper presents a programmable architecture for application versatile fractional-N synthesizer using digitally controlled two data inputs. It is implemented in 0.35μm CMOS process. With 1MHz reference frequency and 2.4GHz VCO it shows programmability in step sizes (18.4kHz to 500kHz), channels selection (64 channels) and output frequency offsets (0 to 37MHz). It has 19mA current consumption@3V, phase noise of –110dBc/Hz@1MHz, resolution of 18.4kHz, settling time < 37μS, divide-by-32/33 Dual Modulus Prescaler (DMP) and 4.2mm² die.

II. DESCRIPTION

Figure 1 [5] shows the block diagram of the system. The output frequency is mathematically derived as:

$$Fout = Fr*M*N + M*Fr*(f/2^n) + A*M*Fr*(d/2^n)$$

Here, n is the number of bits used for data processing by modulus controller. The first and second terms correspond to minimum output frequency limited by hardware design and offset in output frequency controlled by data word f respectively. The last term governs the channel spacing by programmable data word d and the value A provided by channel select block decides the corresponding channel. This is how the implementation of above expression leads to a flexible design. The inherent degree of design freedom in it provides the feature of one design for several applications. Using the following expressions, the input data d and f are provided:

$$\text{Step size} = M*Fr*(d/2^n)$$
$$\text{Offset frequency} = M*Fr*(f/2^n)$$

The accuracy in step size and frequency offset here depends on n, which is hardware limited and can be improved by increasing number of bits.

III. IMPLEMENTATION AND RESULTS

In this implementation, an accumulator based 12-bit first order sigma-delta modulator is used [6]. Two digitally controlled words d and f are input to modulus controller and a control from channel select block is provided. A charge pump LPF (Low Pass Filter) is used to develop control voltage for 2.4GHz VCO LC tank [7]. The VCO output frequency is fed through a differential buffer to high frequency dual modulus divide-by-32/33 prescaler, which is further divided by a divide-by-75 counter. Excluding the RC components of third order loop filter, monolithic realization of this design is achieved using CSM foundry parameters.

The 52-pin QFP (Quad Flat Package) packaged device is mounted on a PCB board for testing. The output pin is connected to HP 8563E Spectrum Analyzer using 50 ohm RF cable and

0-7803-7694-3/03/$17.00 © 2003 IEEE

microstrip line. A 3.0 V DC supply is used. Based on measured results, Figure 2 depicts how step sizes and output frequencies vary with data value of d and f respectively. Output power spectrum response and noise performance are shown in Figure 3 and Figure 4 respectively. Reference noise level is measured as – 110dBC/Hz at 100kHz offset. Loop switching behavior using HP54540 torage Oscilloscope is shown in Figure 5 for a switching of 1MHz and 37MHz respectively. Figure 6 shows modulus controller operation at 1MHz while programmed for minimum mode density of 0.0002 by setting d=1 , f=0 and A=1. This value of mode density corresponds to 200Hz resolution should this synthesizer be implemented with M=1.Table 1 provides measurement summary. In this design, phase noise is limited by the VCO performance. However, this architecture allows enhanced performance using low noise wide tuning range VCO and high order, high number of bits sigma-delta modulator. Figure 7 shows the die microphotograph.

Table 1: F-N PLL Performance Summary

Reference Crystal	999.91kHz
Output Power	-8.42dBm ± 2%
Minimum Channel Spacing (Step Size)	18.4kHz
Channel Spacing Range	18.4kHz to 500kHz
Channels per set of (d, f)	64
Offset Frequency Range	0 to 37MHz
Resolution	18.4kHz (Loop division =2400)
Loop Settling Time	<37μS (step< 0.5MHz)
Phase Noise	-60dBc/Hz@ 1kHz offset -89dBc/Hz @100kHz offset -104dBc/Hz@500kHz offset -110dBc/Hz@ 1MHz offset
Reference Noise	-110dBc/Hz @100kHz offset
Loop Bandwidth	10kHz
VCO Tuning Range	2375MHz-2500MHz
VCO Sensitivity Kvco	133.8MHz/V @1V 233.9MHz/V @ 0.5V

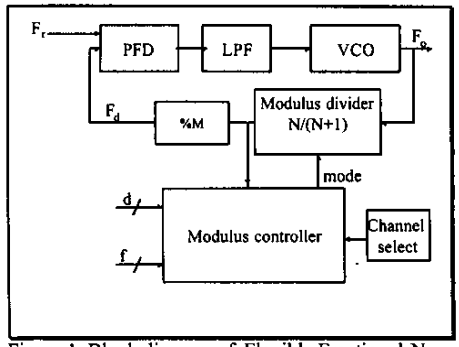
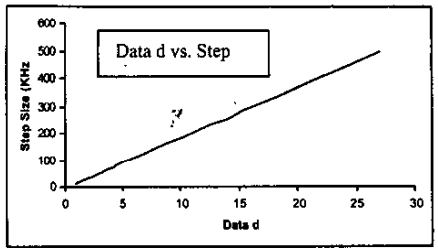


Figure 1: Block diagram of Flexible Fractional-N Synthesizer



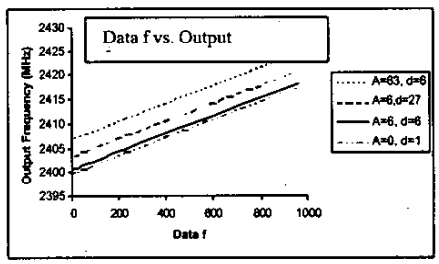


Figure 2 : Input data controlled performance

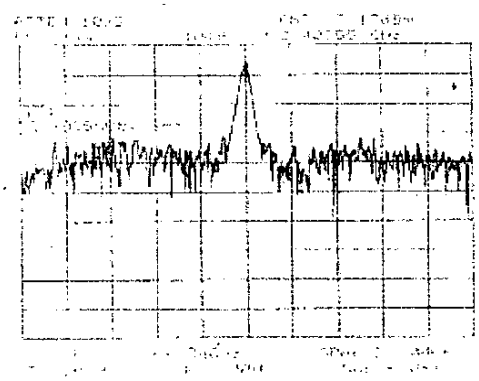


Figure 3: Output power spectrum (A=4,d=27,f=64)

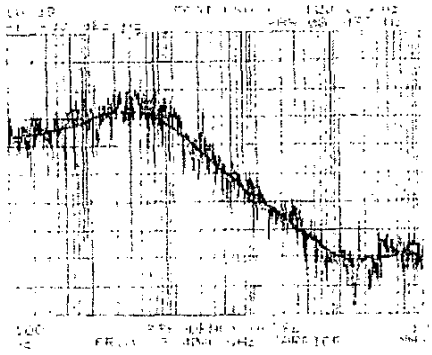


Figure 4 : PLL Noise response

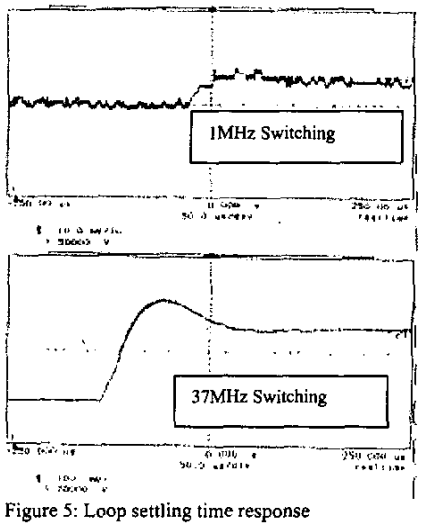


Figure 5: Loop settling time response

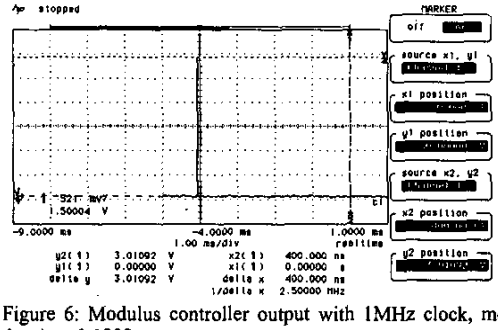


Figure 6: Modulus controller output with 1MHz clock, mode density =0.0002

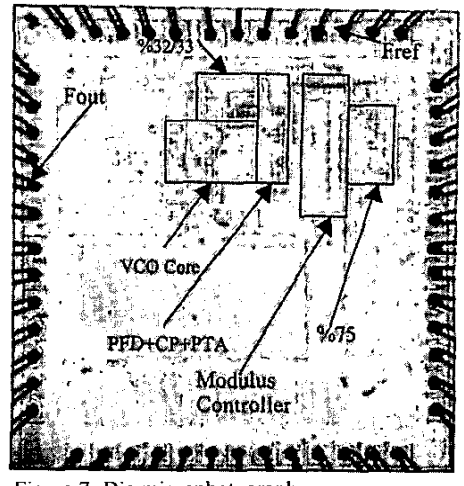


Figure 7: Die microphotograph

ACKNOWLEDGEMENT

Thanks are due to M. M. Aung for assistance in layout and PCB development, to U. Dasgupta, A. Ajjikuttira, R. Singh and S. C. Rustagi for valuable encouragement.

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